

Fig. 1

Fig. 1A Fig. 1B

Fig. 1B

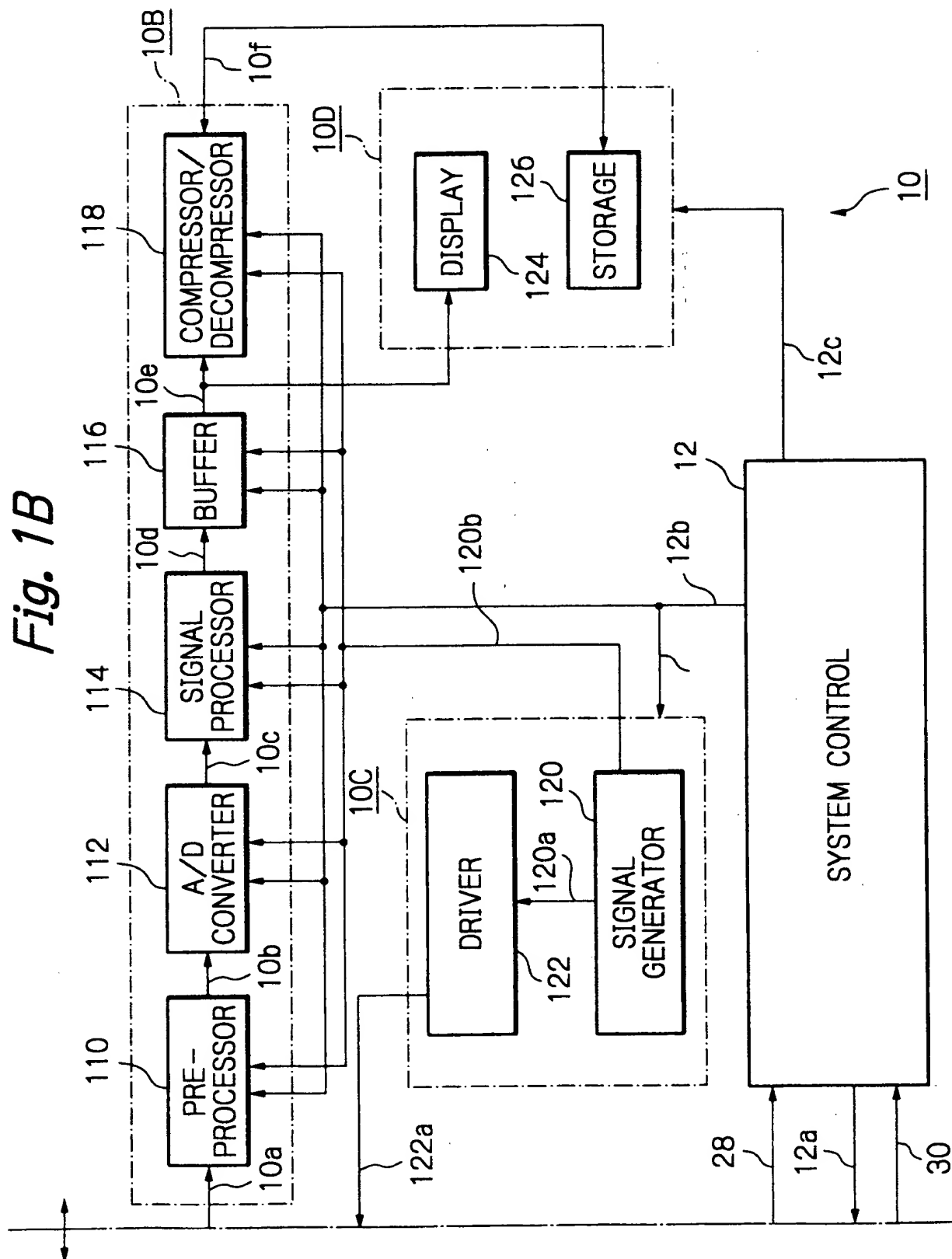


Fig. 2

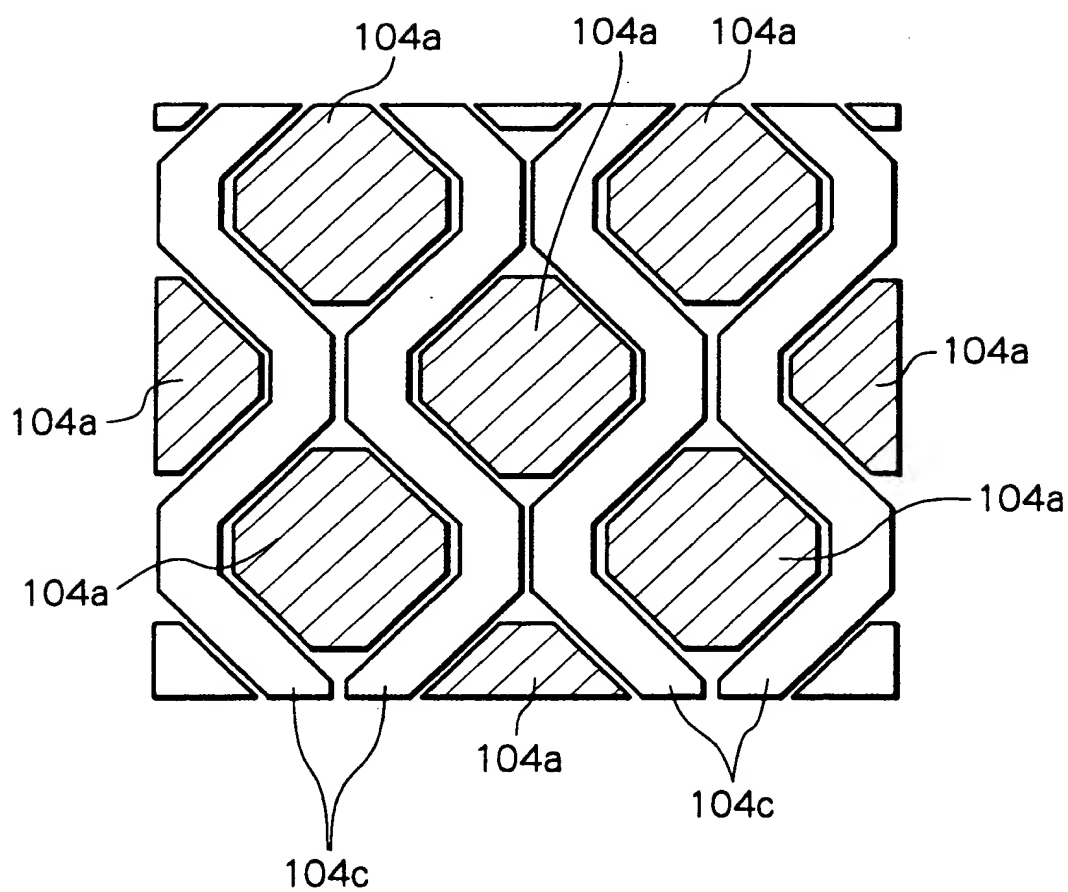


Fig. 3

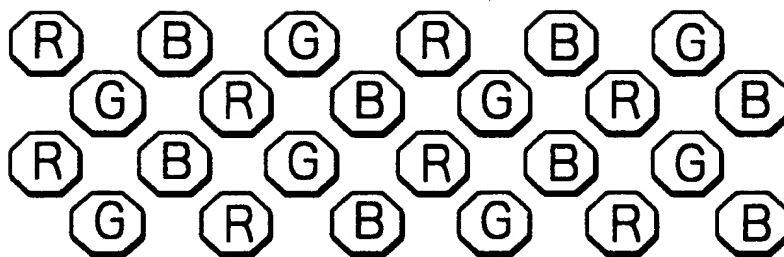


Fig. 5

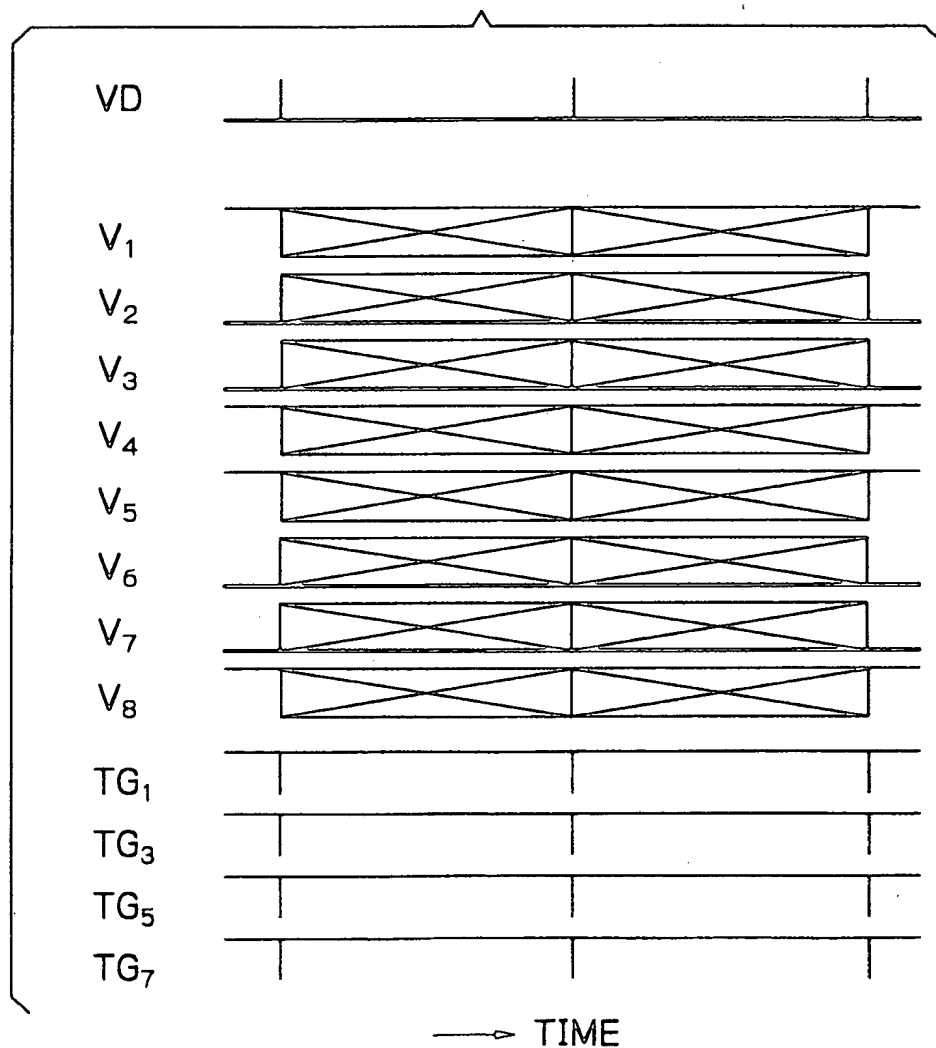
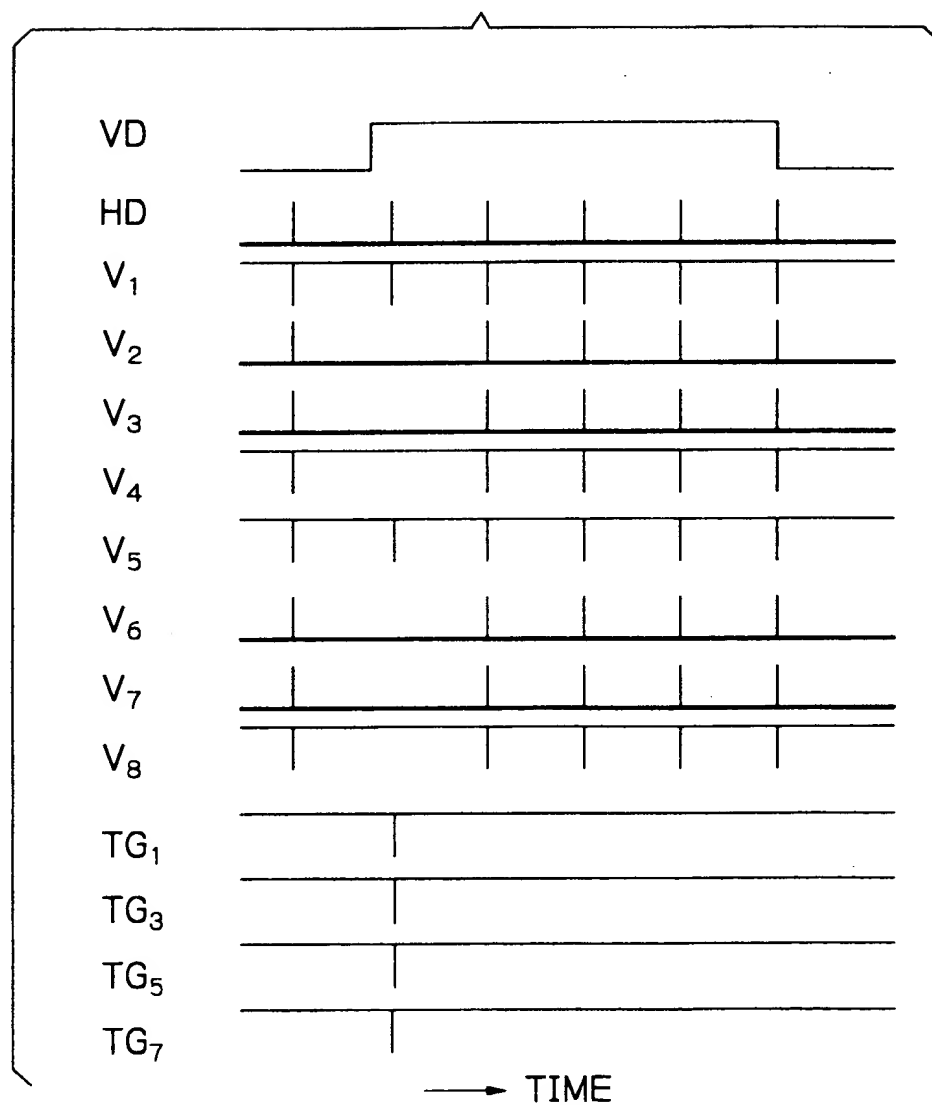


Fig. 6

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Fig. 7

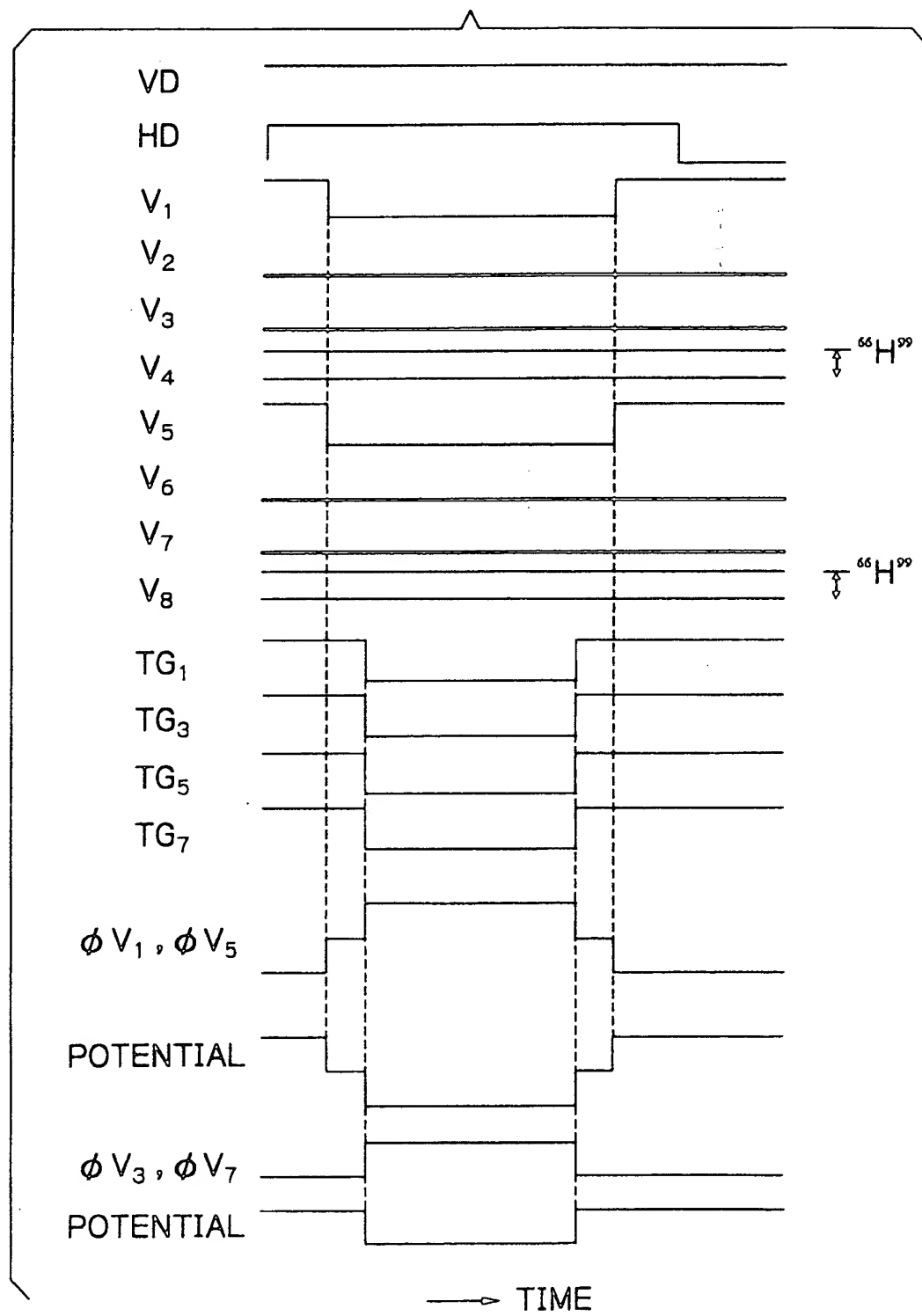


Fig. 8

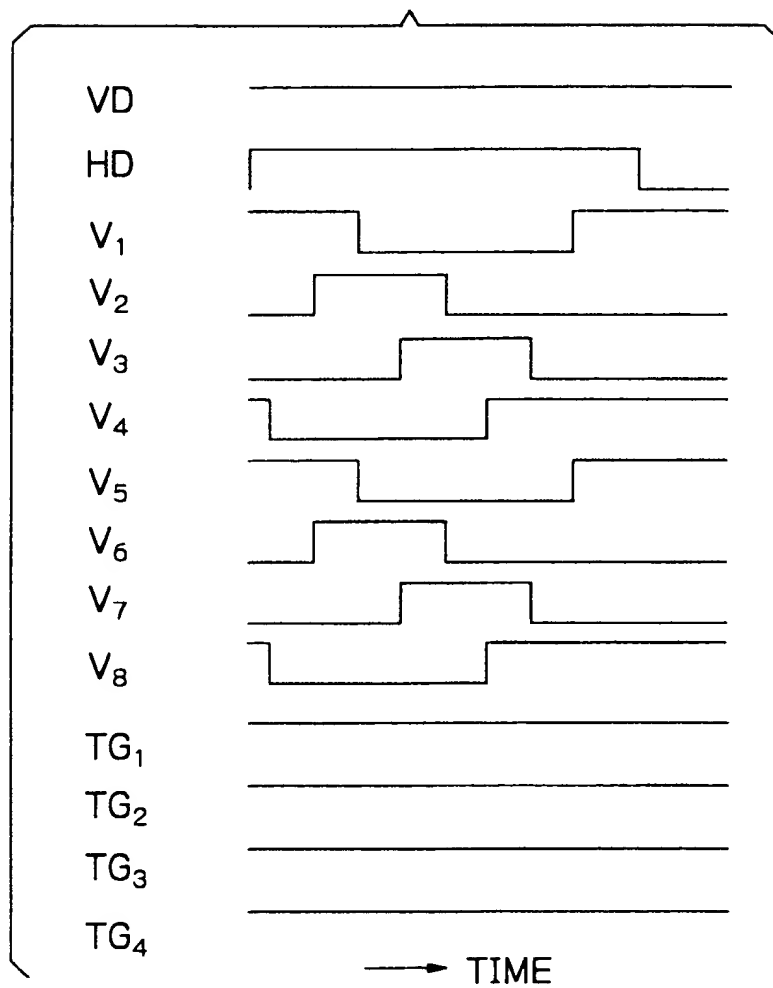
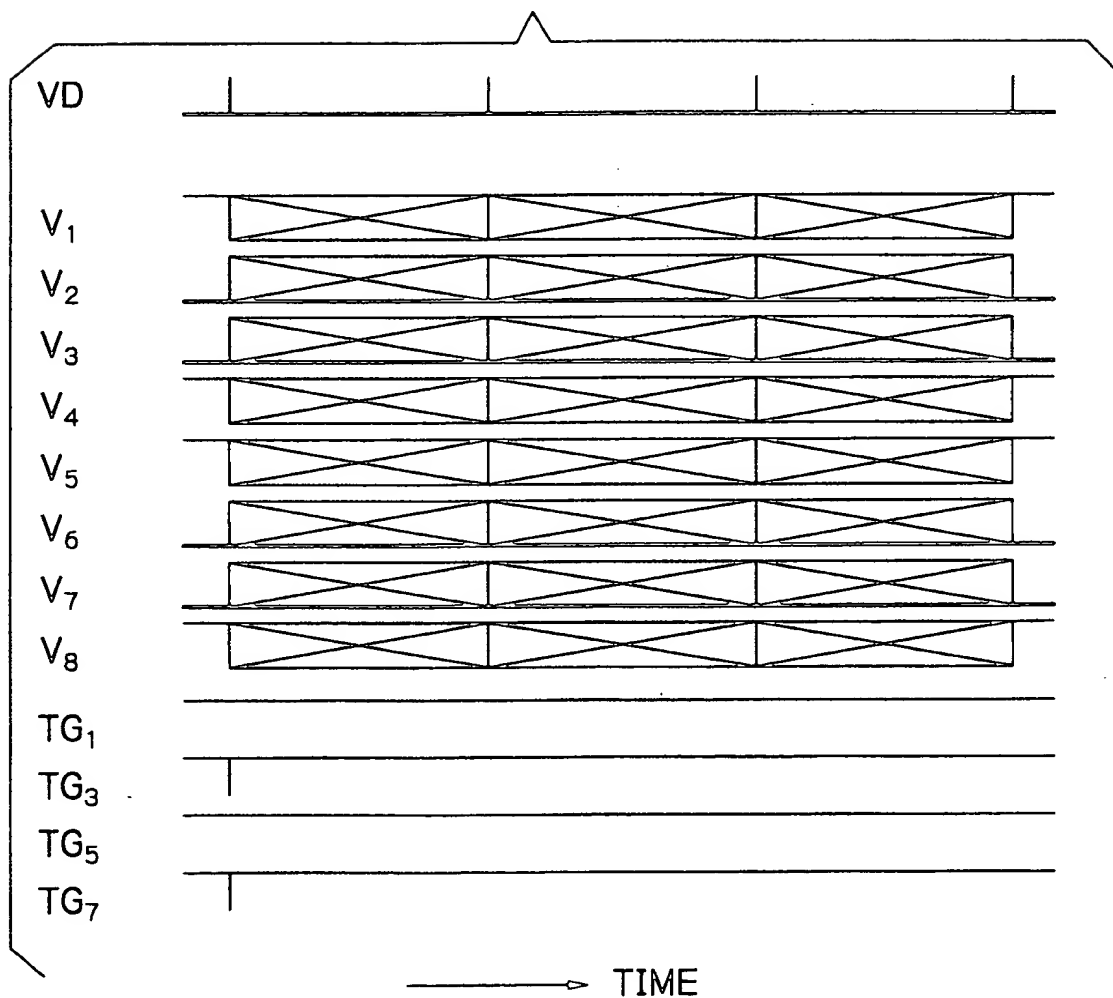


Fig. 9



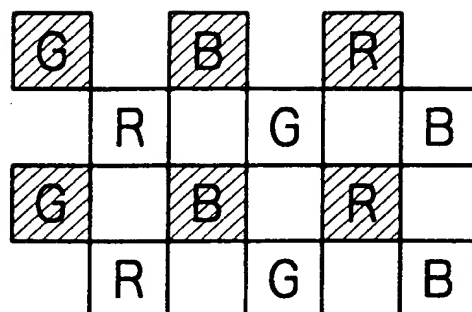
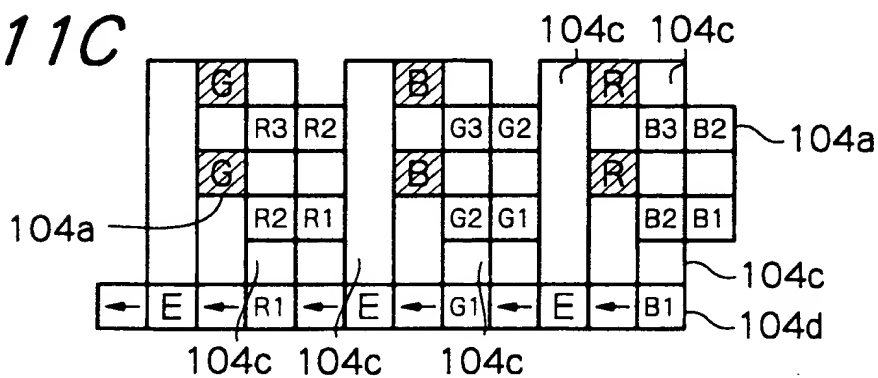
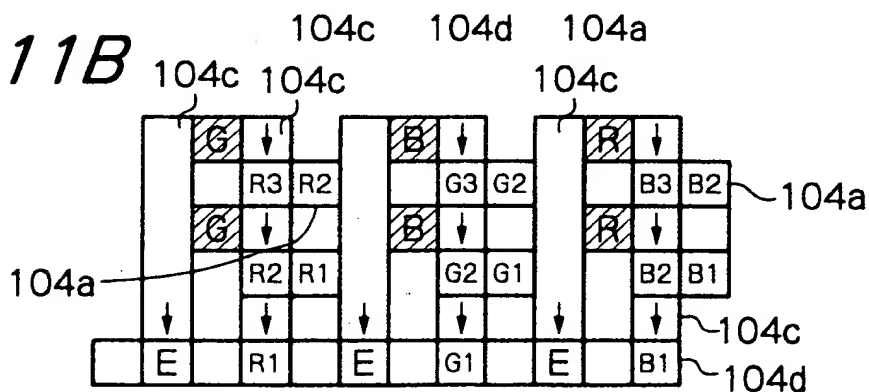
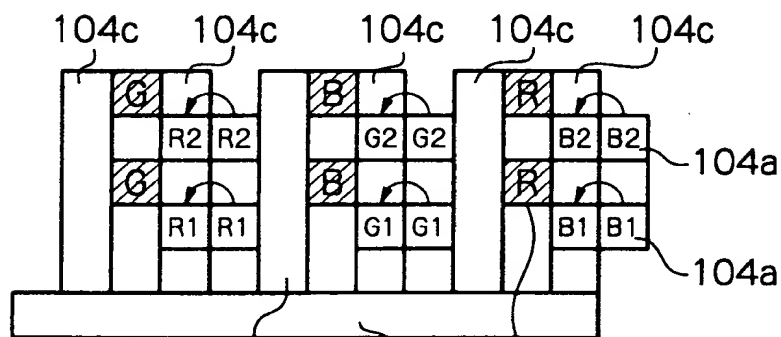
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Fig. 12A

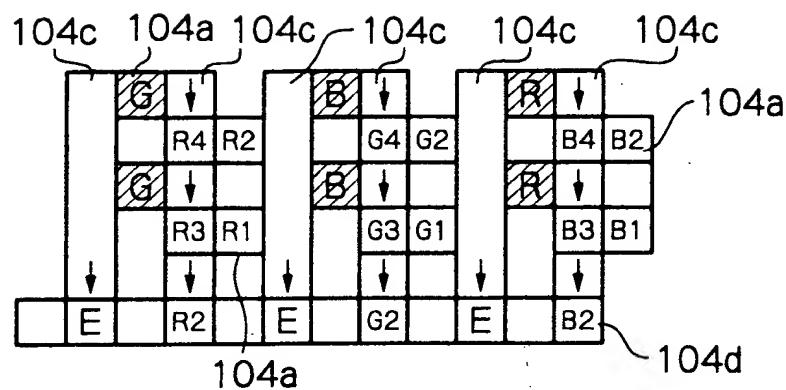


Fig. 12B

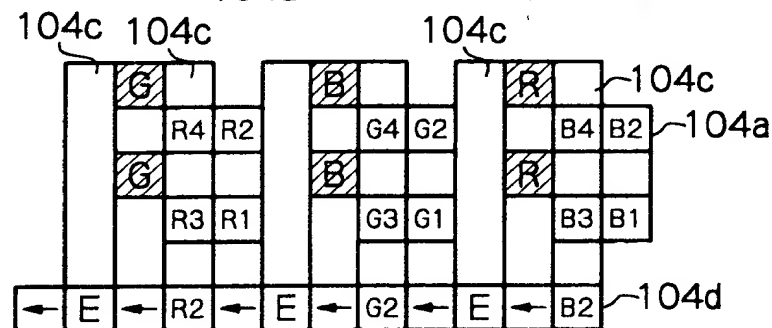


Fig. 13A

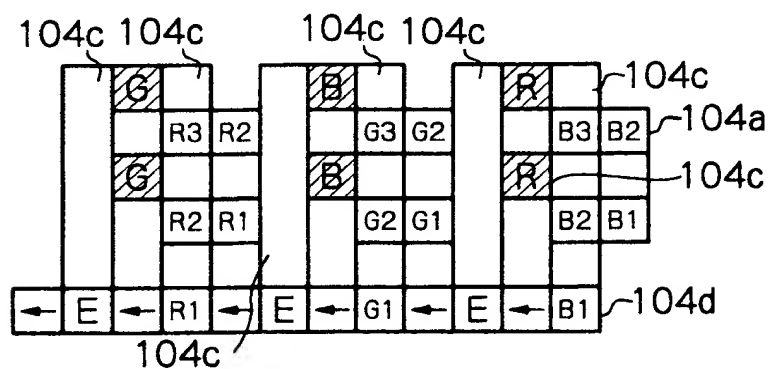
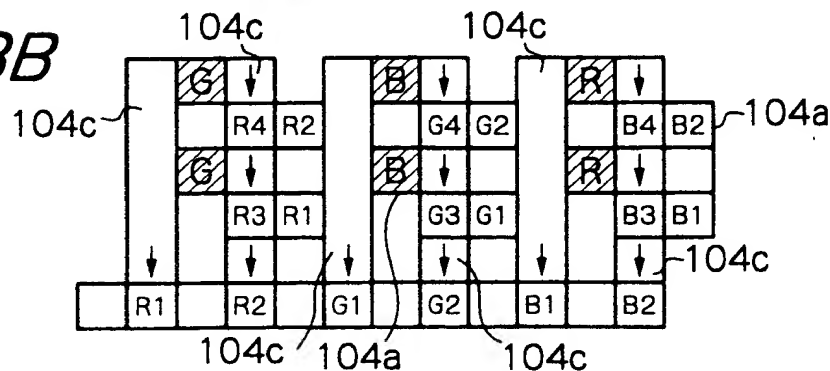


Fig. 13B



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Fig. 14

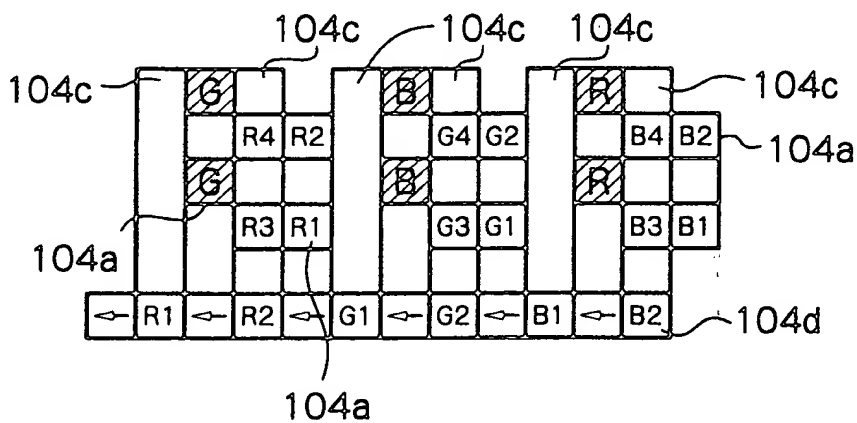


Fig. 15

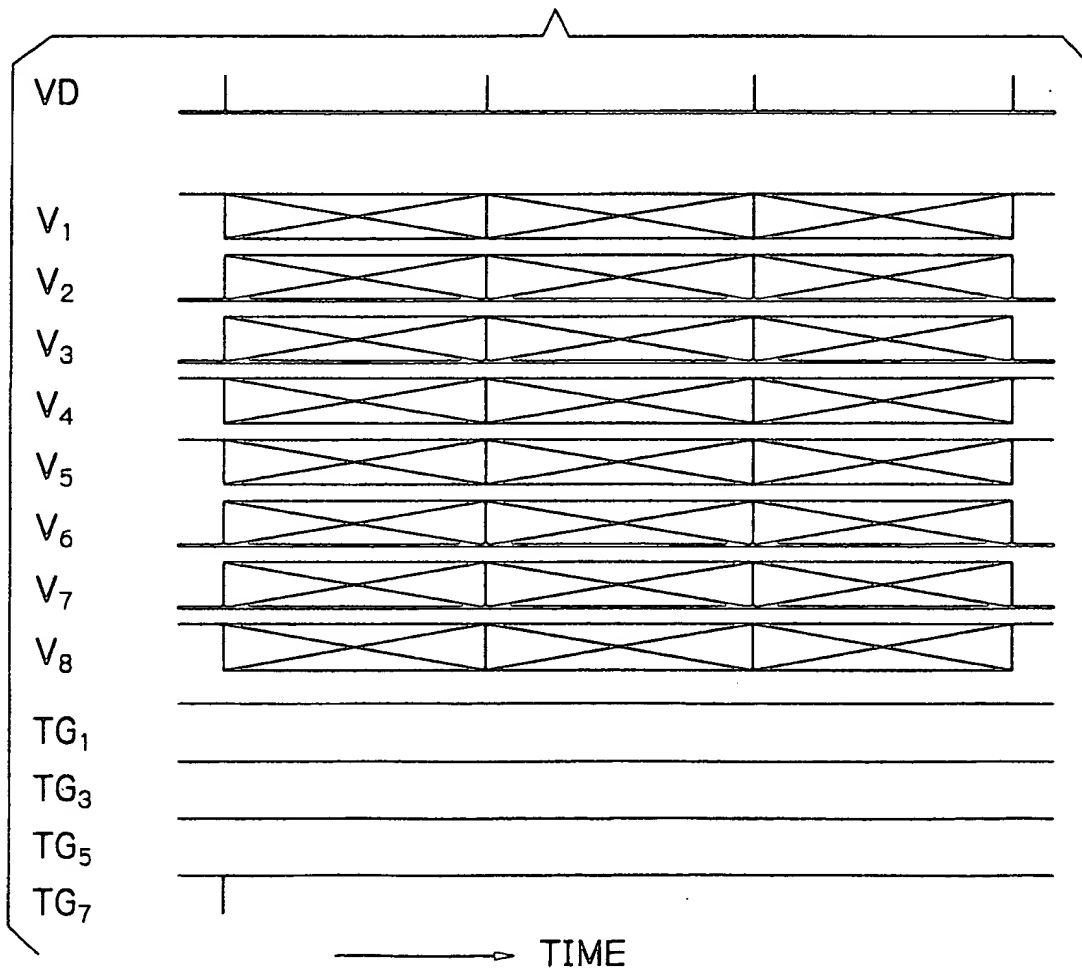


Fig. 16

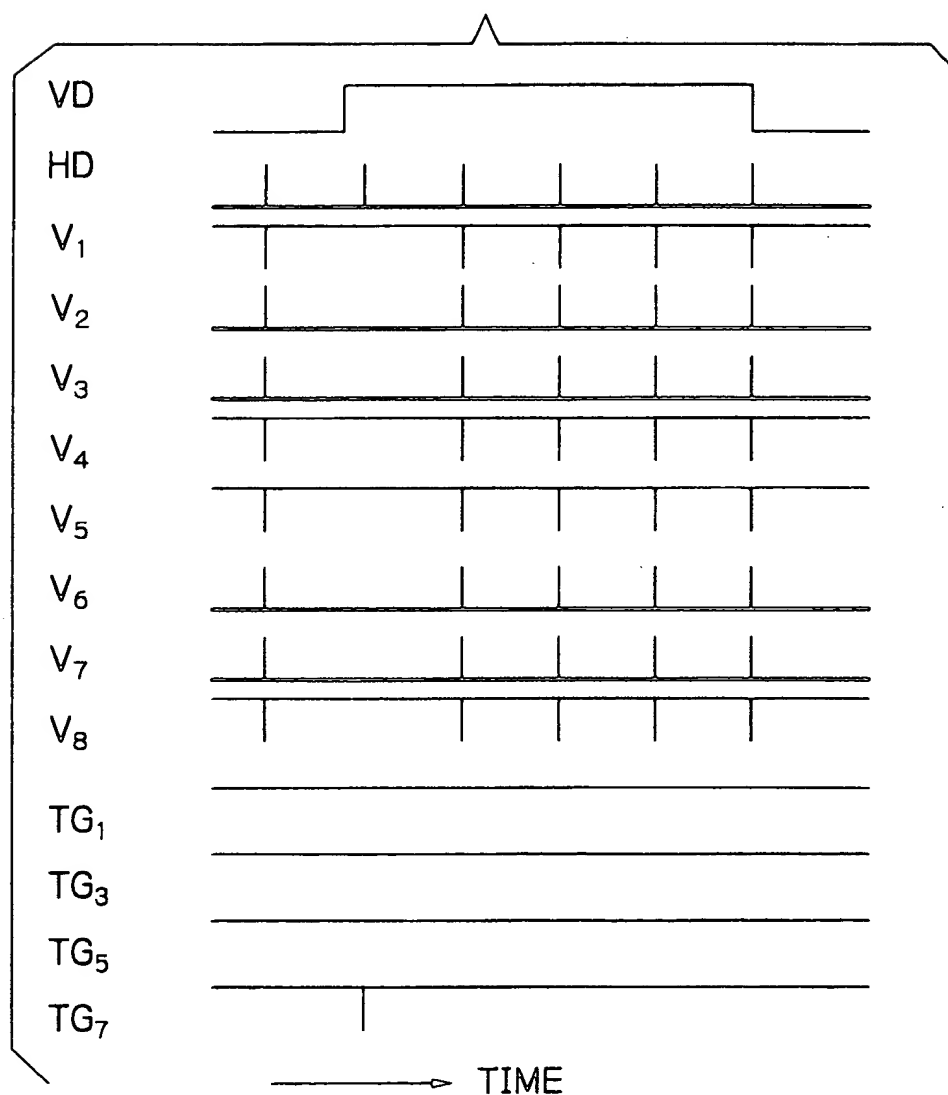


Fig. 17

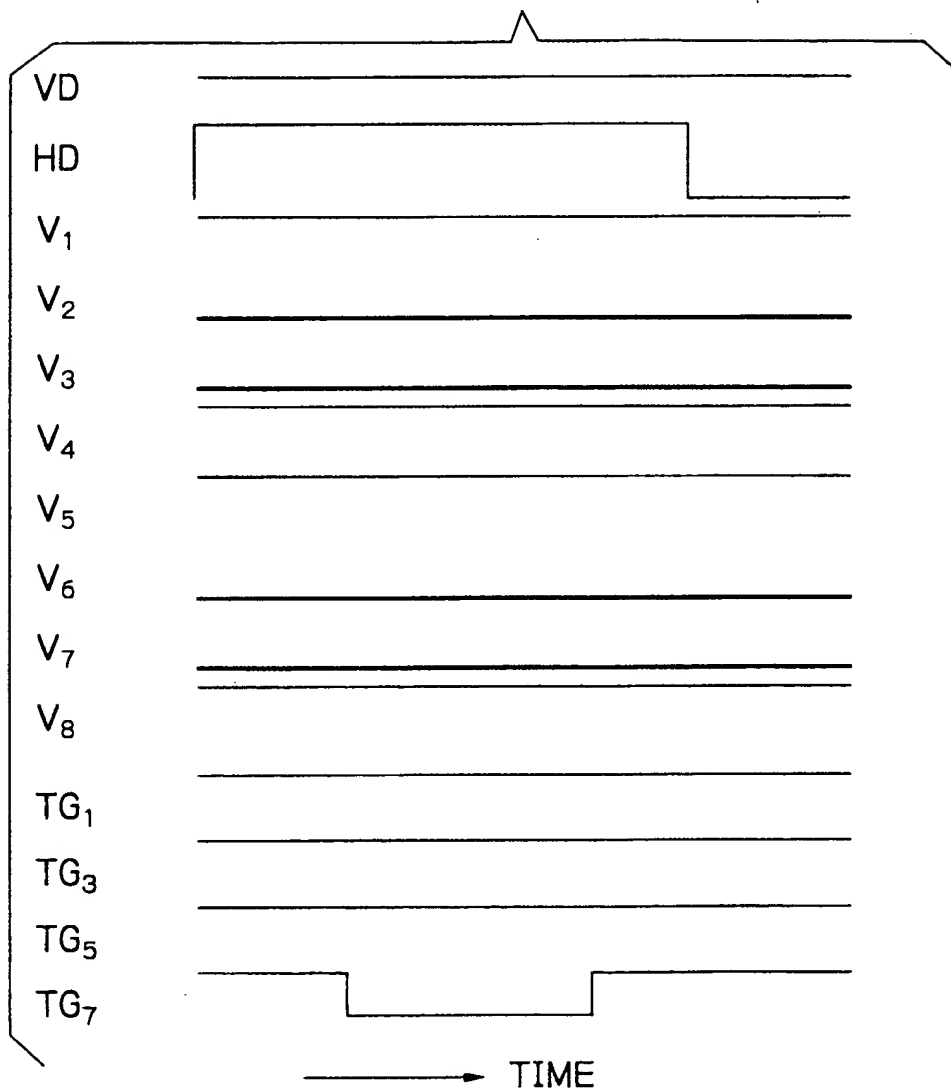


Fig. 18A

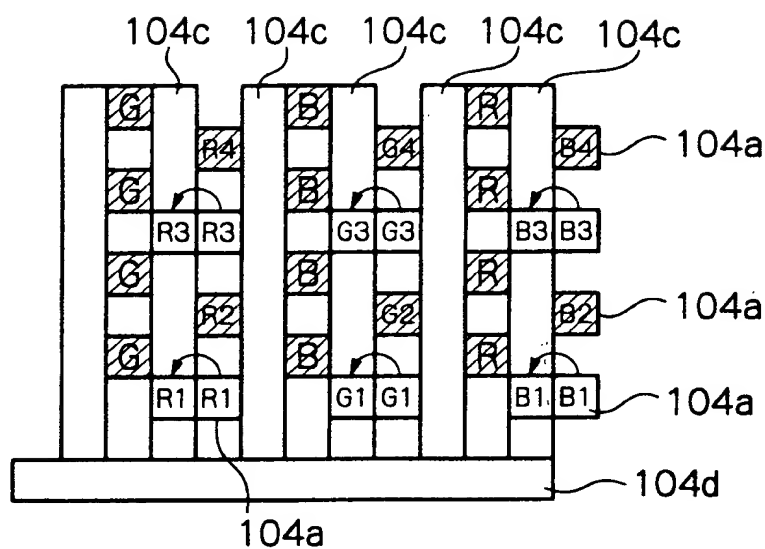


Fig. 18B

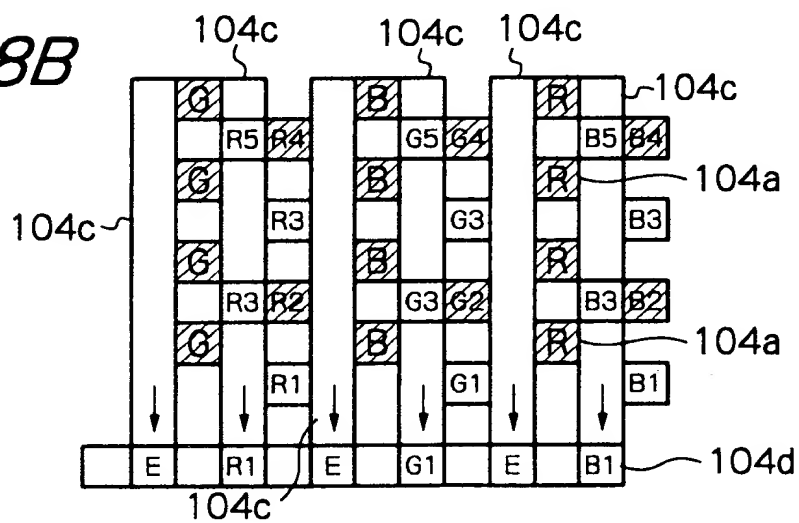
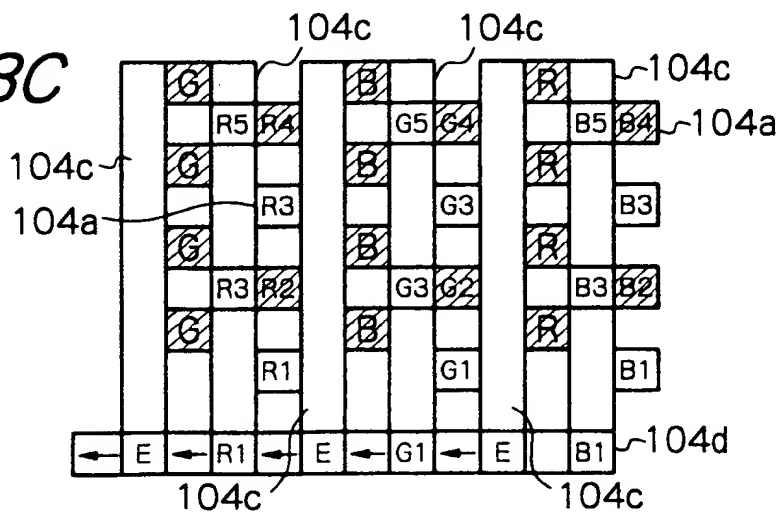


Fig. 18C



The diagram illustrates a 3D NAND memory array structure. It shows a grid of storage cells arranged in rows and columns. The columns are labeled 104c, 104a, 104c, and 104c from left to right. The rows are labeled 104a, 104a, and 104d from top to bottom. The cells are represented by rectangles, some of which are shaded with diagonal lines. The cells are labeled with letters G, R, and B, and numbers 1 through 7. The labels 104c, 104a, and 104d are placed near the corresponding columns and rows. The cells are arranged in a 3x4 grid, with the columns labeled 104c, 104a, 104c, and 104c. The rows are labeled 104a, 104a, and 104d. The cells are labeled with letters G, R, and B, and numbers 1 through 7. The labels 104c, 104a, and 104d are placed near the corresponding columns and rows.

Fig. 20A Fig. 20B

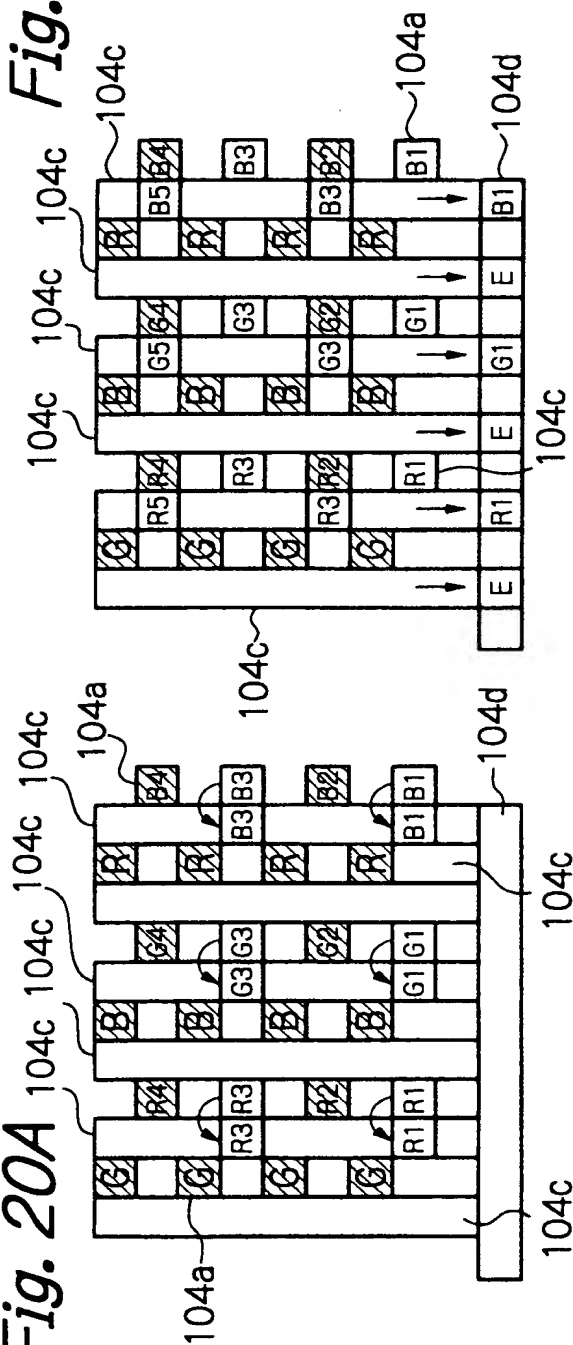


Fig. 20D

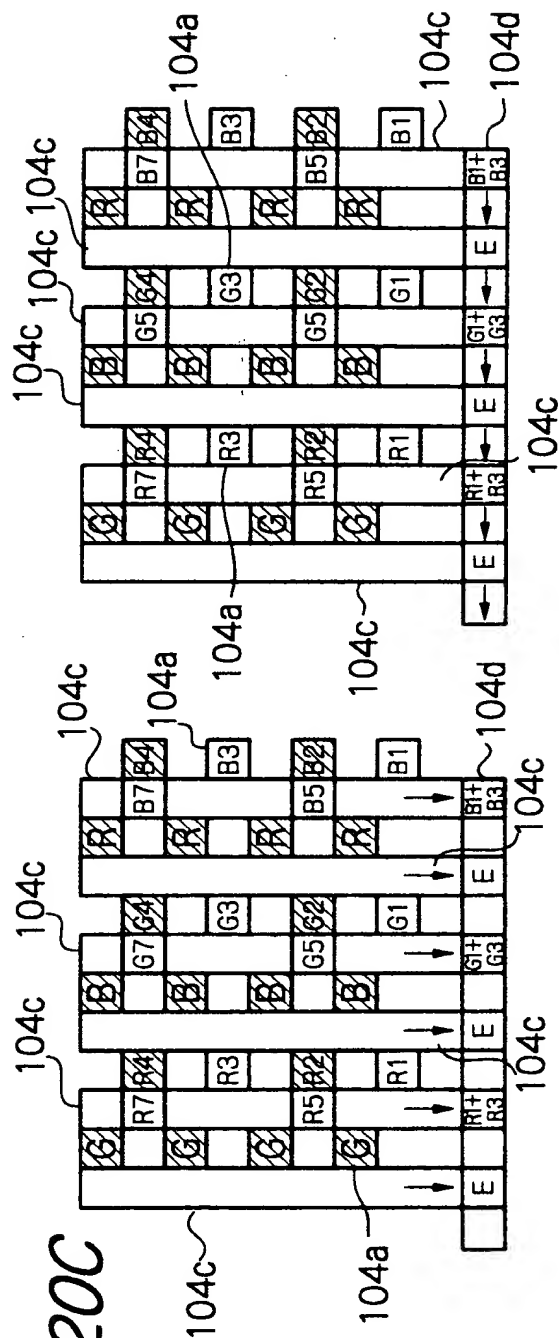


Fig. 20C

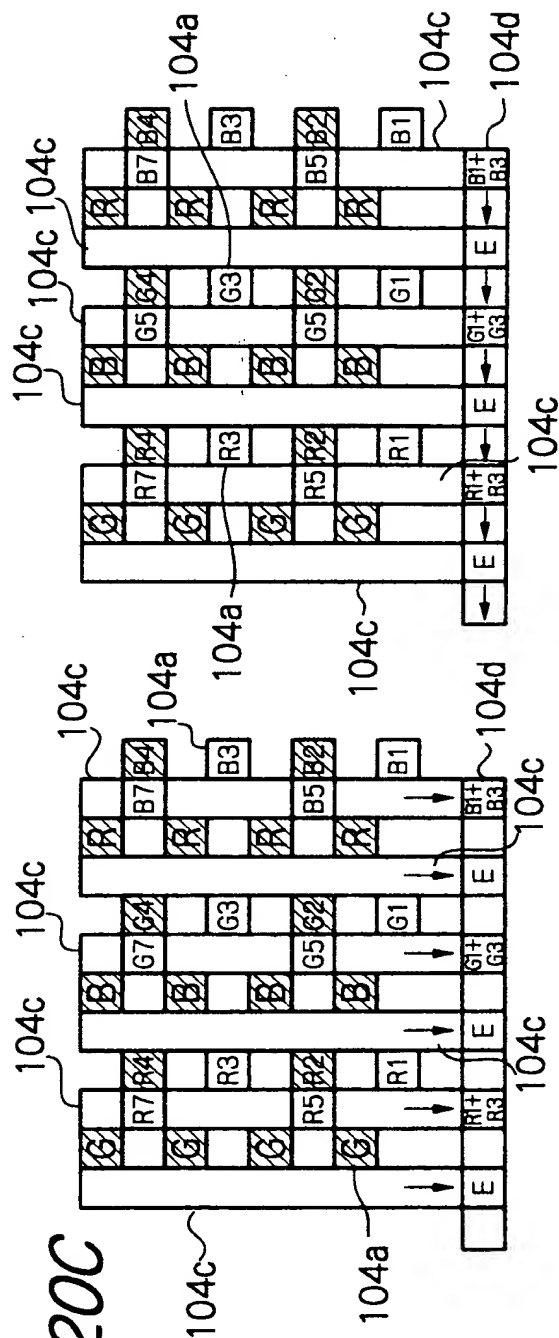


Fig. 21B

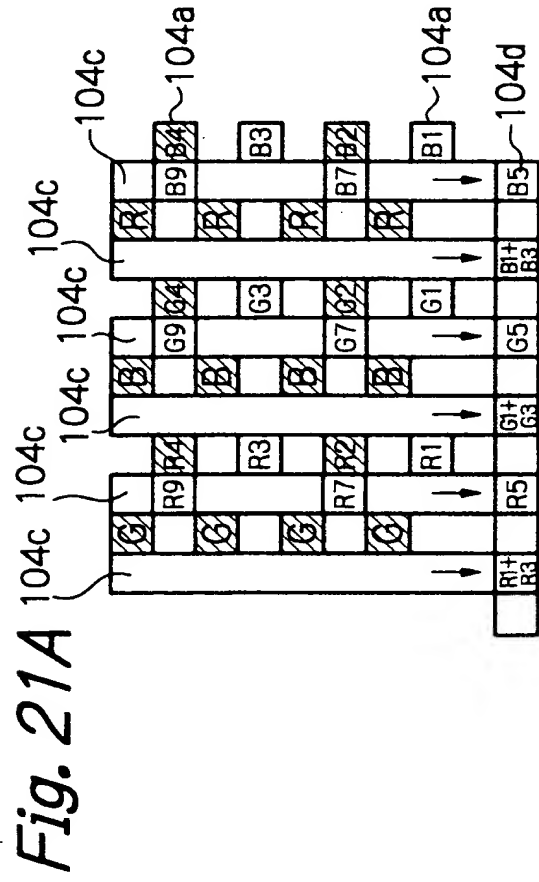
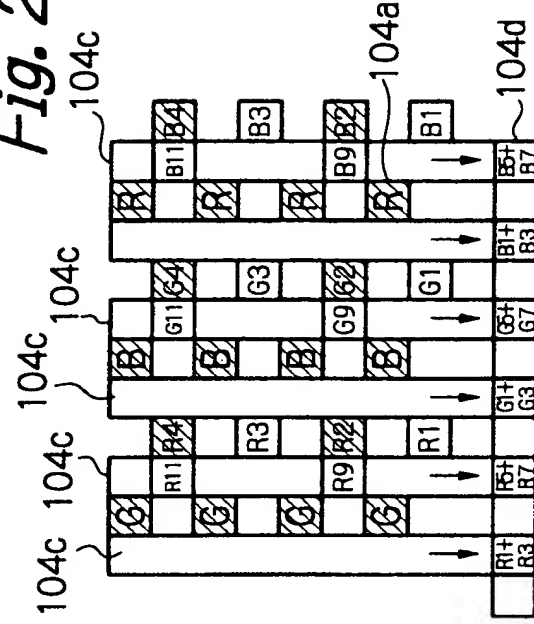


Fig. 21C

